REMARKS/ARGUMENTS

Claims 1-11 and 18-36 are pending in the present patent application. Claims 1, 2, 4-5, 8-9, 18-20, 25-28, 30, 32-33, and 35 have been amended. New claim 36 has been added. No new matter has been added to the new or amended claims. Reconsideration of the claims is respectfully requested.

The Restriction Requirement

Claims 12-17 were canceled in a prior amendment pursuant to a restriction requirement. Applicant reserves the right to pursue these claims in a divisional application.

Rejections of the Claims Based on Prior Art

The office action rejected claims 1-11 as being obvious over U.S. Patent 6,071,775 to Choi et al. in view of U.S. Patent 5,641,696 to Takeuchi. Applicants wish to point out that claims 18-36 are also pending in the present application.

As discussed in the background of the present application, many prior art memory arrays used high temperature oxide (HTO) to form spacers that insulated the gate stack. Contact holes to the drain/source regions were formed using a contact mask and a contact etch. The contact mask was offset from the edges of the gate stacks, as shown in Figure 2, to prevent the HTO spacers from being removed by the contact etch.

The gate-to-contact offset ensured that the HTO spacers remained intact after the contact etch. Because of the gate-to-contact offset, the dimensions of the memory cells were larger. The gate-to-contact offset was increased further to account for effects that were caused when the contact mask was misaligned. See the present application at paragraph 4, pages 1-2.

The present invention avoids these problems. Because the spacer (e.g., nitride) is mostly resistance to the contact etch, the drain and source contacts are self-aligned with respect to the edges of the gate stacks as shown in Figures 3 and 4 of the present application.

Figure 3 in the present application illustrates an embodiment of the present invention. According to this embodiment, a spacer 57/58 is provided to insulate a gate stack 55

of a memory cell transistor. A contact mask 92 is used to define contact holes, and then a contact etch is performed to form the contact holes.

In Figure 3, the contact mask 92 is aligned with the edges of the gate stack. The contacts to the drain and the source regions of the memory cell are formed in the contact holes. At least a portion of spacer 58 remains substantially intact after the contact etch. See the present application at page 7, paragraph 29.

The claims have been amended to further clarify the invention. Claim 28, for example, has been to recite:

> forming a contact mask over the plurality of gate layers that is aligned with edges of the gate layers; and
>
> performing a contact hole etch to form contact holes to drain or source regions of the memory array transistors,
>
> wherein at least a portion of the first spacers are not removed during the contact hole etch such that the first spacers insulate lateral walls of the gate layers in the memory array transistors subsequent to the contact hole etch

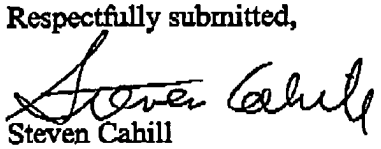
None of the cited prior art references disclose or suggest these features. For these reasons, it is submitted that amended claim 28 is novel and non-obvious over the cited prior art references. The other claims are also allowable.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



Steven Cahill
Reg. No. 44,578

TOWNSEND and TOWNSEND and CREW LLP

Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 650-326-2400 Fax: 415-576-0300
60158499 v1